EXHIBIT 32

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EXHIBIT 33

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EXHIBIT 35

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EXHIBIT 36

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EXHIBIT 37

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EXHIBIT 38

REDACTED

EXHIBIT 39

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

BELL COMMUNICATIONS RESEARCH, INC. (now TELCORDIA TECHNOLOGIES, INC.) Plaintiff, v. FORE SYSTEMS, INC. Defendant.	Civil Action No. 98-586 MMS

PLAINTIFF, BELL COMMUNICATIONS RESEARCH, INC.'S REPLY BRIEF IN SUPPORT OF ITS CLAIM INTERPRETATION ANALYSIS AND IN OPPOSITION TO THE ERRONEOUS CLAIM INTERPRETATION ADVANCED BY DEFENDANT, FORE SYSTEMS, INC.

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I. INTRODUCTION

Over 100 years ago, the Supreme Court warned of the pitfalls of narrowing claims based on a patent's written description or prosecution history: "[I]f we once begin to include elements not mentioned in the claim in order to limit such claim . . . , we should never know where to stop." *McCarty v. Lehigh Valley R.R. Co.* , 160 U.S. 110, 116 (1895). Fore's claim construction ignores the Supreme Court's words in *McCarty,* and the body of Federal Circuit precedent endorsing this view, by improperly reading modifiers and elements of preferred embodiments into the claims.

Fore candidly admits that it has chosen its interpretations to "crystallize the issues relating to Fore's noninfringement and invalidity defenses." *See* F. Br. at 6.[1] In so doing, Fore biases its claim construction analysis, as seen in Fore's consistent attempts to improperly read narrowing modifiers and preferred embodiments into claim terms. As demonstrated below, this biased approach violates the basic tenants of claim construction.[2]

II. ARGUMENT

A. Fore Improperly Attempts to Import Narrowing Limitations from the Patent Specifications Into the Claims

1. Fore's claim interpretations violate the rule that narrowing modifiers are not read into unmodified general terms

Narrowing modifiers are not added to otherwise general terms standing unmodified in a claim. *See* B. Br. at 26. Thus, for example, in *Bell Communications Research, Inc. v. Vitalink Comm. Corp.*, 55 F.3d 615, 621-22 (Fed. Cir. 1995), the Federal Circuit held that the claim term "associating" covered both explicit and implicit association. And, in *Specialty Composites v. Cabot*

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[1] In this reply brief, citations to Bellcore's opening brief are to B. Br. at __. Citations to Fore's opening memorandum are to F. Br. at __. Additional Exhibits are provided in Bellcore's Supplemental Appendix of Exhibits in Support of Its Claim Interpretation Analysis.

[2] Claims must be construed independent of the accused products. *Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1580 (Fed. Cir. 1991).

Corp., 845 F.2d 981, 987 (Fed. Cir. 1988), the court similarly refused to limit the claim term "plasticizer" to external plasticizers. *See also Pirelli Cable Corp. v. Ciena Corp.*, 988 F. Supp. 424, 436 (D. Del. 1997) (Schwartz, J.) ("input/output" port of optical coupler "should be read as broadly as possible within the parameters that the claim language permits" and can be either bidirectional connection or connection supporting only input or output connection).

Fore's claim interpretations consistently violate this basic claim construction rule. As one example, Fore improperly attempts to narrow the generic term "bit stream" in '306 patent claim 1 to a "serial bit stream," *See* F. Br. at 10. Similarly, Fore wrongly attempts to narrow the term "gateway" in '080 patent claim 6 to a "uni-directional gateway." *See* F. Br. at 40. Other examples of Fore's improper attempts to narrow the claims are discussed below.

2. Fore improperly attempts to limit the claims to the preferred embodiments described in the patent specifications

Fore also improperly limits claim terms to particular embodiments shown in the patents. "References to a preferred embodiment, such as those often present in a specification, are not claim limitations." *Laitram Corp. v. Cambridge Wire Cloth Co.*, 863 F.2d 855, 865 (Fed. Cir. 1988). That a specification describes only one embodiment does not require that each claim be limited to that embodiment. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985).[3]

Fore consistently violates this rule in its claim interpretation. For example, as to the '306 patent, Fore wrongly insists that a payload field must be "100% filled," simply because that is what the preferred embodiment discloses. *See* F. Br. at 12. Similarly, for the '768 patent, Fore contends

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[3] *Karlin Tech. Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 973 (Fed. Cir. 1999) (preferred embodiment showing "highly specialized threads" did not limit the ordinary meaning of a "series of threads"); *Virginia Panel Corp. v. MAC Panel Co.*, 133 F.3d 860, 866 (Fed. Cir. 1997) (refusing to limit unmodified term "reciprocating" to linear reciprocation since "it is well-settled that device claims are not limited to devices which operate precisely as the embodiments described in detail in the patent").

that "reconstructing" means "aligned, latched and converted from serial to parallel form," simply because those additional functions are performed for a disclosed embodiment. *See* F. Br. at 28.

B. In Attempting to Raise Validity Issues In Support of Its Claim Interpretation Fore Fails to Meet Its Burden of Establishing Invalidity by Clear and Convincing Evidence

1. Fore ignores its burden of proving invalidity by clear and convincing evidence

Fore similarly ignores the law in advancing invalidity arguments in support of its claim interpretations. First, Fore ignores its burden of proof to establish invalidity by clear and convincing evidence. *See, e.g., United States v. Telectronics, Inc.*, 857 F.2d 778, 785 (Fed. Cir. 1988). Indeed, despite Fore's several invalidity arguments, (*see, e.g.*, F. Br. at 13, 42 and 58-61), nowhere does Fore address its burden of proof—a burden which Fore does not come close to meeting on any of these arguments. This lack of evidentiary support reveals Fore's invalidity arguments as simply another, poorly disguised attempt to improperly limit the claims to a preferred embodiment to advance its noninfringement contention.

2. Fore fails to address numerous factual issues regarding the alleged lack of enablement of the '306 and '080 patents

In presenting its non-enablement arguments, (F. Br. at 13, 42, and 50) Fore simply ignores the various underlying questions that must be addressed in considering the enablement issue. Enablement under 35 U.S.C. § 112 is a question of law based on underlying factual issues. *Bruning v. Hirose*, 161 F.3d 681, 686 (Fed. Cir. 1998). To be enabling, a "patent must contain a description sufficient to enable one skilled in the art to make and use the claimed invention" without undue

experimentation. Telectronics, 857 F.2d at 785.[4] *See also SRI Int'l*, 775 F.2d at 1121 (a patentee need not describe every conceivable embodiment of the invention).

Fore neither mentions nor discusses any of these issues in advancing its non-enablement positions. Rather, Fore's arguments consist of unsupported allegations that do not even begin to meet its burden of proof.

3. Fore's allegation that '080 patent claim 6 is indefinite is flawed

Fore's indefiniteness argument (*see* F. Br. at 42) is likewise flawed. Initially, "[a]mbiguity, undue breadth, vagueness, and triviality are matters which go to claim validity for failure to comply with 35 U.S.C. § 112 ¶ 2, not to interpretation or construction." *Intervet Am., Inc. v. Kee-Vet Labs., Inc.*, 887 F.2d 1050, 1053 (Fed. Cir. 1989). *See also CCPI, Inc. v. American Premier, Inc.*, 966 F. Supp. 276, 283-84 (D. Del. 1997) (Schwartz, J.).

Even were this not so, Fore's indefiniteness argument is flawed. Definiteness under 35 U.S.C. § 112, ¶ 2, is a question of law requiring the Court to inquire if one skilled in the art would understand the bounds of the claim in light of the specification. *Personalized Media Comm. LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 702,705 (Fed. Cir. 1998). The claims, read in light of the specification, need only "reasonably apprise those skilled in the art of the scope of the invention." *Miles Lab., Inc. v. Shandon, Inc.*, 997 F.2d 870, 875 (Fed. Cir. 1993).

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[4] Enablement is not precluded even if some experimentation is needed—the amount of experimentation must, however, not be unduly excessive. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384 (Fed. Cir. 1986). Factors to consider in determining whether undue experimentation would be required include: (1) the quantity of experimentation needed, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988).

Although Fore contends that the claim language of '080 patent claim 6 "according to predetermined system guidelines" is indefinite, it offers no evidence to support that assertion.[5] Rather, Fore argues that no "guidelines" are offered in the '080 patent. This is incorrect. In fact, the '080 patent describes guidelines for selecting a set of spanning trees: a) providing sufficient communications capacity; b) eliminating bottlenecks at or near a network root; c) reducing traffic passing through other nodes in the network; and d) choosing between disjoint spanning trees and parallel spanning trees. *See, e.g.*, A*28 at col. 6, lines 11-56.

The flaws in Fore's indefiniteness argument are further shown by Fore's use of a cropped quote from Dr. Sincoskie's publication. See F. Br. at 42-43, F. Ex. 12 at 7. In fact, the complete quote makes it clear that the "challenging open question," on which Fore bases its argument, is the selection of "an **optimal** set of spanning trees." Claim 6, however, does not require the selection of an optimal set of spanning trees.[6]

4. In alleging invalidity of '954 patent claim 9, Fore ignores the law that a patent claim is only inoperable when it is totally incapable of achieving a useful result

In arguing that its claim construction must be adopted or claim 9 of the '954 patent would be invalid as inoperable (*see* F. Br. at 58-61), Fore likewise ignores the law regarding inoperability. A patent claim is inoperable only when it is totally incapable of achieving a useful result. *Brooktree Corp. v. Advanced Micro Devices, Inc.*, 977 F.2d 1555, 1571 (Fed. Cir. 1992); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1269 (Fed. Cir. 1986); *Envirotech Corp. v. Al George, Inc.*, 730

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[5] As in *PMC*, the evidence offered by Fore "is relevant, if at all, only to the sufficiency of the written description to enable the practice of the invention of the claims, which is a ground of invalidity under § 112, ¶ 1," not the definiteness requirement of § 112, ¶ 2. *PMC*, 161 F.3d at 706. Fore, however, does not argue non-enablement with respect to this claim provision.

[6] Moreover, the article echoes the teaching of the '080 patent that by applying guidelines such as network communication capacity, e.g., "maximum traffic on a given trunk," heuristics can be developed for selecting a set of spanning trees for a particular network.

F.2d 753, 762 (Fed. Cir. 1984). Even if an invention "has only limited utility and is only operable in certain applications" it is not invalid for lack of utility. *Envirotech*, 730 F.2d at 762. Fore, at most, advances one particular hypothetical condition under which the claimed invention may or may not operate effectively. That one hypothetical is of no moment or relevance, since even Fore does not contend that the claimed invention is totally incapable of achieving a useful result.

Thus, Fore's approach in advancing its claim interpretation is legally without foundation. It violates the basic rules of claim construction followed by the Supreme Court, the Federal Circuit, and this Court. Having addressed these fundamental flaws in Fore's claim interpretation analysis, Bellcore will now focus on specific errors in Fore's constructions.

C. Fore Improperly Construes the Claims of the Patents in Suit

1. The '306 patent

a. Fore's proposed claim construction is based on its misrepresentation of the claimed invention

Fore's "Overview of the Technology" (F. Br. at 7) completely mischaracterizes the operation of the '306 patent. Fore's distortion is illustrated in its Diagram 2, where it purports to illustrate the "generating" and "filling" process implemented by the framer circuits 52, 53 (Fig. 4) described in the patent. *See* F. Br. at 8. Diagram 2, however, is totally unsupported by the patent specification. It erroneously depicts three full frames *simultaneously* existing within some unexplained circuitry between points A and B. The diagram shows two data packet sources operating simultaneously on two of the frames as the frames pass by the sources.

Nothing in the '306 patent specification supports this bogus depiction of the operation of the framer circuits. Bellcore correctly described the operation of the framer circuits in its opening brief, at p. 6. As noted there, the framer circuits are shown in Fig. 12 (A* 11). Data bytes representing frames with empty payload fields are generated by Frame Byte ROM 224. The bytes, generated one

byte at a time in bit-parallel format, are output on bus 219 and are converted to a bit-serial format on line 206. The train of empty frame bytes is applied to input line 202 of the next-connected framer circuit, which operates to insert packetized data from one or more source devices in place of the data representing the empty payload fields of the frames.

The empty frame generating framer and the packet inserting framer circuits *are part of the same transmitter*. As is clear from the patent specification, the framers perform the operations of generating empty frames and filling the empty frames with packetized data on a byte-by-byte basis in "real time." As the empty payload field bytes are presented to TRI 218, they are either passed to the output (if no packet data is available) or blocked (if packet data is to be inserted). At no time is there ever an entire frame of data, let alone three entire frames of data as shown in Fore's Diagram 2, present in a framer circuit.

b. Fore wrongly interprets claims 1 and 3

i. "*generating a bit stream*"

Again, Fore improperly reads the narrowing modifier "serial" into the term "bit stream." Thus, Fore's claim interpretation cannot stand. Fore's proposed construction is tainted by its misleading description of the '306 technology. The phrase "generating a bit stream" in claims 1 and 3 pertains to the operation of the framer that generates the sequence of empty frame signals.

The first step of claims 1 and 3 in fact pertains to the "internal" bit stream produced by the framer that generates the sequence of empty frames. As shown in Fig. 12 of the '306 patent (A* 11), which Fore chooses to ignore, the sequence of empty frames is generated on "parallel bus" 219, one byte at a time. At this point, the frames are formatted as a *parallel* bit stream, not as a serial bit stream. The bit stream is converted to a serial format when it is fed to the adjacent framer and then is reformed into a parallel bit stream for processing by that framer.

Thus, as the specification clearly shows, the train of empty frames exists, at different times, both as a parallel and as a serial bit stream. Claims 1 and 3 characterize it generically as a "bit stream" and are properly interpreted to include both.[7]

ii. ***"frame timing information"***

Fore wrongly contends that "[f]rame timing information is one or more bits that indicate the beginning of a frame." F. Br. at 11. The '306 patent defines this phrase, however, as a "frame alignment word." A*14 at col. 6, lines 61-65. A binary "word" is always more than one bit.[8] Fore frankly states that it desires a claim construction that will support its position on invalidity, i.e., it wants to argue that the claim covers prior art systems that include one framing bit per frame. The indication of the beginning of a frame in those systems is provided only by inspecting a predetermined bit pattern made up of the single framing bits contained in a whole sequence of frames.

The '306 patent claims, however, call for the frame timing information to be contained in the transmission overhead field *of each frame*. Fore's proposed claim construction therefore does not hold water. A single frame bit is not timing information capable of "indicating the beginning of a frame."

iii. ***"empty payload field"***

Fore interprets this phrase to mean that "a frame's payload has zero data in it." F. Br. at 11. Fore incorrectly explains that Fig. 2 shows that "[t]he frames with empty payload fields are generated before any source data is available for insertion into the frames." F. Br. at 12.

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[7] Note the distinction in claim drafting where, for example, asserted claim 13 of the '768 patent specifically states "a serial bit stream." Not so the claims of the '306 patent.

[8] Contrary to Fore's misleading analogy to written words, such as the article "a," being an English "word," a single bit cannot be a binary "word." A "word" is a sequence of bits or bytes. Ex. M, A*143-144.

This proposed claim construction appears to be a repetition of Fore's position based on its misleading Diagrams 2 and 3, i.e., that an entire empty frame must be generated before it is available to be filled with packet data from a source input. As shown above, the '306 framer circuits do not work that way. Empty payload bytes are generated in sync with the payload field portion of the frame.[9] Thus, Fore's proposed construction (iii) is flawed because it is inconsistent with the description of the invention.

iv. ***"filling the empty payload fields in said frames"***

Fore argues that "filling the empty payload fields in said frames" requires "(1) that a complete empty frame is first created, and (2) that, after creation, the frame's empty payload is 100% filled with a packet."

Step (1) of Fore's claim construction is erroneous and must be rejected because, as explained above, empty payload fields are generated by a first framer one byte at a time and are filled by a second framer byte-by-byte in real time, i.e., as the empty payload field is being generated. It is thus impossible for a complete empty frame to exist before it is filled.

In step (2) of its proposed construction, Fore appears to be asking the court to read a "one packet per frame" and a "one packet per payload field" limitation into the claims. This aspect of the proposed claim construction is based on nothing more than the specific payload field and packet sizes described for the preferred embodiments in the '306 patent. Nothing in the claim, however, requires 100% filling, as argued by Fore. Clearly, Fore is reading in a modifier based on its noninfringement-driven arguments.

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[9] TRI 218 (A* 11) selects the empty bytes if no complete packet is present in a FIFO memory. TRI 218 blocks the empty bytes and TRI 220 passes the packet bytes when a complete packet is available.

Although Fore's enablement argument, discussed above, is less than clear, Fore apparently contends that the term "*[f]illing the empty payload fields in said frames*" means that the term is limited to putting only a single packet into a payload field. As shown above, Fore's enablement argument is legally flawed and Fore offers no evidence that one skilled in the art would not be enabled by the '306 patent to put more than one packet into a single payload field.[10]

v. "***such that data in packetized format from any of said sources is written into any available payload field of any of said frames***"

Here again, Fore wants the court, for non-infringement purposes, to construe the claims to require insertion of only a single packet in each frame so that systems that insert multiple packets per frame are not within the literal language of the claim. As shown above, importing details of the described embodiments into a claim, when the plain language of the claim does not so warrant, defies the basic rules of claim construction.

Claims 1 and 3 require each frame to have "an empty payload field." Frames that have several empty payload fields literally have "an empty payload field," as claimed. Fore's attempt to have the Court rewrite the claims to require each frame to have "one and only one empty payload field" must be rejected. Fore cites no authority that requires patents to describe every embodiment within the scope of the claims, because no such rule exists.[11] An applicant need not describe more than one embodiment of a broad claim to adequately support that claim. *Ethicon Endo Surgery, Inc. v. United States Surgical Corp.*, 93 F.3d 1572, 1582 (Fed. Cir. 1996).

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[10] Fore simply ignores the fact that, during prosecution of the application leading to the '306 patent, the applicants explained to the Examiner that the invention would cover implementations having multiple packets in a single frame payload. Ex. 6 at A*82.

[11] Fore's argument (Brief, p. 13) that the '306 patent does not enable placing multiple packets in a frame is irrelevant. Claims 1 and 3 do not claim a process for inserting multiple packets in a frame. The claim language is nonetheless broad enough to cover a system that inserts more than one packet in each frame.

vi. ***"filling. . .from a plurality of sources which have access to the bit stream. . .such that data in packetized format from any of said sources is written into any available empty payload field of any said frames. . .for transmitting data simultaneously via said bit stream"***

Fore's attempt to link multiple limitations together, omitting words where convenient, confuses and rewrites the claim. Fore contends that the above quoted language requires that two or more empty frames are filled at the same time by different data sources. This interpretation is inconsistent with the teachings of the specification. The term "simultaneously" simply does not modify "filling." Rather, it clearly modifies "transmitting."

Fore points to its Diagram 3 in support of this claim construction. Diagram 3 is essentially identical to Diagram 2 and is equally misleading. Fore contends that the words "simultaneously" used in the preamble and body of claim 1 support the diagrams. This contention is incorrect because, as noted above, it is impossible for one whole frame, let alone two whole frames, to be present in a framer circuit or in a series of framer circuits. Thus, Fore's proposed construction is simply wrong.

The word "simultaneously" appears in the last line of each of claims 1, 3, and 4 and also in the preamble of claim 1. It means that data from a plurality of sources, i.e., packets, is interspersed into a common transmission stream. *See* B. Br. at 30. When data from several sources is carried in a single transmission signal it is commonly understood that such source data is simultaneously transmitted. For example, a conventional telephone T-1 trunk line "simultaneously" transmits voice data from twenty four telephones by multiplexing them together. The '306 patent relates to "dynamic" multiplexing and uses "simultaneously" in the same sense to indicate that data from several sources is transmitted within the same transmission stream.

c. Fore's proposed construction of claim 4 incorrectly identifies the "corresponding structure" pursuant to 35 U.S.C. § 112, ¶ 6

Fore proposes (F. Br. at 19) that the *entire* framer circuit of Fig. 12 be regarded as the structure in the '306 specification that corresponds to the "generating means" of claim 4. Such a

proposed construction is unacceptable because the Fig. 12 circuit functions both as the empty frame generator and as the packet inserting circuit (Col. 16, lines 12-22) while the "generating means" deals only with the empty frame generation functions.[12]

Bellcore has identified only those components of Fig. 12 dealing with empty frame generation as corresponding to the "generating means," namely frame Byte ROM 224, tristate device 222, control 210, and timing generator 209. Bellcore's position is the only one that makes sense because 35 U.S.C. § 112, para. 6 implicates only those structural elements shown in the specification which are involved in performing the claimed function. *Unidynamics Corp. v. Automatic Prods. Int'l, Ltd.*, 157 F.3d 1311, 1319 (Fed. Cir. 1998).

Fore does the same thing with the "processing means" element of claim 4 by including the FIFO memories along with the packetizers. The claim language recites only the function of "processing data from a plurality of sources into packet format." The FIFO memories store packets *after* they have been formed. They are not involved in packetizing.

Fore's interpretation of the "inserting means" as requiring *multiple* framers of the type shown in Fig. 12, with the framers arranged in a daisy-chain configuration, seeks to add still further unnecessary limitations to claim 4. Bellcore's construction accurately designates only those elements of a single Fig. 12 framer that are involved in the claimed "inserting" function. B. Br. at 36.

Fore's position also ignores the second embodiment shown in Fig. 10. That embodiment performs the claimed "inserting" function using only a single framer 160. The framer 160 receives the "train of frames" from framer 162 and receives packets from a plurality of sources via FIFO 158. Thus, the corresponding structure is not restricted to that shown in Fig. 4.

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[12] Fore's suggestion to classify the entire Fig. 12 circuit as part of the "generating means" is clearly nothing more than an attempt to create a non-infringement position by adding unnecessary structural limitations to the claim.

Accordingly, Bellcore's § 112, para. 6 claim construction conforms with the '306 patent specification, while Fore's construction ignores the patent specification and is contrary to law.

2. The '768 Patent

a. Fore's proposed construction of claim 13 improperly seeks to limit the claim to the disclosed embodiment

Fore wrongly asks the court to read limitations into the preamble of claim 13 that call for a particular method of *forming* the serial data bit stream that is operated on in the claimed "method for demultiplexing." In its proposed construction (i), Fore says that the preamble "requires each frame of the serial bit stream that is being demultiplexed *to have been formed* by interleaving all eight bit bytes of two or more contributory frames." F. Br. at 25. The example given by Fore implies that the "contributory frames" incorporated in the bit stream must be originated *separately* and then combined by single-byte interleaving "with no gaps or pauses or breaks" in the interleaving pattern. F. Br. at 25-26. Fore asserts that "the serial bit stream of claim 13's alleged invention consists of multiple 'low level signal frame structures' (lower-order SONET frames) that are multiplexed byte-by-byte into a single higher-order frame." F. Br. at 27 (emphasis added).

The preamble of claim 13 contain no limitations relating to a particular method of forming the bit stream. The claim specifies a particular byte sequence without specifying where or how the bytes originated. The word "multiplexed" is not mentioned in the claim.[13] There is no requirement that the "contributory frames" be originated separately and later byte-interleaved to form the "serial data bit stream."

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[13] In its proposed construction (iii) (F. Br. at 29), Fore also asks the court to construe step (a) of claim 13 to require that the serial data bit stream be "multiplexed." The step of multiplexing is plainly not included in step (a), or anywhere else in claim 13, and cannot be part of any proper interpretation of step (a). Fore's proposed construction (vi) also attempts to add a multiplexing limitation into claim 13, and is likewise improper and must be rejected.

The preamble simply states that the continuum of interleaved data bytes making up the stream is "derived from" a plurality of identically-formatted contributory frames. Thus, the bytes of the contributory frames could have been *originated* in a transmitter in the sequence F1A, F1B, F1C, F2A, F2B, F2C, etc. Clearly, the A, B and C bytes can be interleaved *as they are being generated* and the resulting bit stream will meet the requirements of claim 13's preamble (assuming the bytes meet the specified size and formatting requirements). Thus, Fore's proposed construction is wrong.

b. Fore erroneously interprets other terms in claim 13

i. "*byte*"

Fore improperly attempts to limit the term "byte" to an 8-bit byte. *See* Fore Br. at 27. Once again, Fore's attempt to narrow the plain language of the claim violates controlling Federal Circuit precedent, which precludes such a construction.[14] Fore's construction is also inconsistent with standard dictionary definitions making it clear that a "byte" is a group or sequence of bits operated on as a unit by a computer. *See* Ex. N, A*147, 150, 152-153.

ii. "reconstructed byte"

Fore says that the preamble phrase "reconstructed bytes" means bytes that have been "aligned, latched, and converted from serial to parallel form." F. Br. at 28. Fore's construction inexplicably and improperly introduces the additional method steps of aligning, latching, and

[14] Fore's attempt to limit the generic claim term "byte" limited to an "8 bit byte" is also improper in its interpretation of the claim limitation "*accumulating data bits from said serial stream to form bytes having the same predetermined number of bits as do said interleaved data bytes.*" Clearly, had Bellcore intended to define a byte as an 8 bit byte, it could have done so rather than generically claiming that the bytes had the same "predetermined number of bits" without limiting the claim by specifying that number. Fore also improperly reads a multiplexing function into this limitation.

converting into the preamble.[15] In the context of claim 13 "reconstructing said data bytes" means simply identifying the byte groupings, e.g., an 8-bit byte grouping, of the transmitted frame.

iii. "comparing bit patterns from a contiguous plurality of said output reconstructed bytes with bit patterns known to have comprised a like plurality of bytes of each of said contributory frames"

Fore's proposed construction (vi) is incorrect because it would attribute a meaning to step (e) of claim 13 that is inconsistent with the '768 patent specification. The "contiguous plurality" of bytes that is compared in step (e) is a contiguous plurality of bytes that is known to exist in the transmitted higher-order bit stream, but that *cannot* exist in any contributory frame. The bytes of the contributory frames are *interleaved* within the transmitted higher order frame, which means that none of the bytes in the contiguous pattern were contiguous or adjacent in a contributory frame.

For example, the "contiguous pattern" of bytes compared in the described embodiment is F1 F2 F2. As shown in Fig. 2 (A* 21), the F1 byte is part of contributory frame N, the first F2 byte is part of contributory frame 1, and the second F2 byte is part of contributory frame 2. None of the bytes in the compared "contiguous plurality" of bytes belongs to the same contributory frame, let alone is part of a similar contiguous byte sequence within that frame.

Fore's proposed construction (vi) also wrongly requires "bit patterns from two or more *adjacent* reconstructed bytes to be compared with bit patterns known to have been present in two or more *adjacent* bytes in *each* of the contributory frames." F. Br. at 31. This is clearly incorrect because the patent describes a comparison operation that compares bytes that are contiguous

[15] Bellcore essentially agrees with Fore's proposed construction (v), except that step (d) of claim 13 does not include the limitation "latched," which implies a particular structural implementation. Once again, Fore's proposed claim construction seeks arbitrarily to read limitations from the specification into the claim in order to narrow its scope. Such a claim construction is unwarranted and must be rejected.

(adjacent) within the reconstructed byte sequence, but which do not occupy such a position within their respective contributory frames.

The phrase "bit patterns known to have comprised a like contiguous plurality of bytes of each of said contributory frames" in step (e) of claim 13 means that the contributory frames each have a plurality of bytes like the bytes included in the compared "contiguous plurality" of bytes. The phrase cannot mean, as Fore would have the Court believe, that the compared contiguous plurality must exist within each contributory frame. The requirement for byte interleaving obviously make such an arrangement impossible.

iv. "effecting in response to said second signal discontinuation of the provision of said first signal"

Fore's proposed construction (vii) improperly describes step (g) of claim 13 in the context of "searching." In the '768 patent, comparator 39 actually continues to search for F1 bytes, but its ability to signal a match is disabled. A* 28, col. 5, lines 36-40. Step (g) of claim 13 is properly interpreted to mean inhibiting the generation of further first signals. B. Br. at 43.

3. The '080 Patent

Fore's interpretation of the '080 patent claim 6, based on its asserted noninfringement positions, is particularly transparent. Here again, Fore reads limitations into claim 6, attempts to restrict claim 6 to the preferred embodiment, and in some instances, rewrites limitations, wholesale.[16]

a. Fore repeatedly misrepresents the Federal Circuit's decision in *Bell Communications*

Contrary to Fore's assertions (F. Br. at 43, 45, 46, 48), in *Bell Communications*, the Federal Circuit did not construe the terms "spanning tree" and "drop list," and did not "hold" that "multiple

[16] Fore also misrepresents certain Bellcore positions. For example, contrary to Fore's representations, Bellcore agrees that a packet includes both source and destination addresses. Also, Bellcore agrees that claim 6 includes separate "assigning" and "associating" steps.

LANs are connected by means of 'bridges,' each of which are themselves [sic] composed of two paired 'gateways.'" The description of these terms are, in fact, found only in the court's "Background" discussion. 55 F.3d at 616-17. The court's claim construction holdings were limited to the preamble term "said packet including a source address and a destination address" and to the "*assigning*" and "*associating*" limitations.[17] *Id.* at 621-622.

b. Fore incorrectly interprets claim 6

i. "*gateway*"

Contrary to Fore's assertions, the term "*gateway*" is not restricted to a uni-directional device. As explained above, Fore's construction violates the vast body of precedent against reading narrowing modifiers into claim terms and reading the preferred embodiment into the claims. As recited in claim 6, the term "gateway" is simply a device that interconnects two networks, and there is no basis to limit this claim term to a uni-directional gateway.

ii. "*source devices*" and "*destination devices*"

"Source devices" and "destination devices" are devices that send and receive packets, respectively. Once again, Fore attempts to read a narrowing modifier into those terms, seeking to transform them to "end-user source devices" and "end-user destination devices." There is no basis to do so. Bellcore defined these devices broadly, and Fore cannot restrict these limitations simply by pointing to the preferred embodiment, or to portions of the '080 specification that merely identify examples of source and destination devices. Depending on how a network is configured, devices other than "end-user devices" may very well send or receive packets.

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[17] Moreover, Fore's oversimplistic post office analogy ignores Federal Circuit's holding that the "associating" step includes both explicit and implicit association.

iii. "***according to predetermined system guidelines***"

As explained above, Fore's indefiniteness argument is both legally and factually flawed. Moreover, there is no particular set of spanning trees required by claim 6. Claim 6 is directed to a method of efficiently transmitting packets in a system of interconnected networks using any selected set of spanning trees. Thus, the claimed method will work no matter what spanning trees are selected. As explained in the '080 patent, the ability to identify spanning trees in a network was known. Accordingly, those skilled in the art would have known how to select multiple spanning trees in a network following predetermined guidelines such as those identified in the '080 patent.

iv. "***assigning, by said source device, one of said trees to broadcast said packet***" and ***broadcasting said packet by said source device through the system on one of said trees***"

Fore wrongly contends that packets are "broadcast" to all gateways in the system or to all end-user devices. *See* F. Br. at 45, 48. The method of claim 6, however, does not require sending packets to all gateways, or to all end-user devices in the system. Also, the last two steps of claim 6 (steps (ii) and (iii) indicate that a gateway can inhibit forwarding of a received packet, thus preventing packets from reaching all gateways or all end-user devices in the system. Fore's proposed claim construction would read these steps out of the claim and would therefore be improper. Thus "broadcasting" simply means transmitting on a tree in the system and does not require transmission to all gateways or all end-users.

v. **"if said gateway does not process packets having said identifier, inhibiting forwarding of said packet; otherwise, inserting said source address in the corresponding one of said lists associated with said identifier"**

Fore interprets step (ii) of claim 6 to mean that "following the execution of the first inhibit or forward decision, the source address of any forwarded packet is always added to the source address list corresponding to the spanning tree assigned by the source device and identified by the spanning tree identifier." Fore admits, however, that this interpretation is "not enabled by the

specification." First, even Fore acknowledges that a claim scope that is not enabled, should not be adopted. To violate this principle, having argued it affirmatively against other patents, undermines the credibility of Fore's argument.

Second, Fore's argument is wrong. Step (ii) of claim 6 simply means that if the "receiving gateway does not process packets having said identifier", i.e., if the gateway is not in the spanning tree identified by the packet identifier or derived from information in the packet, it "inhibit[s] forwarding" of the packet, i.e., the packets are dropped. Otherwise, the source address list for the spanning tree is updated to include the source address from the arriving packet.[18] Bellcore's interpretation is enabled because one of ordinary skill in the art would have known how to add a source address to a list. Indeed, thus function was executed in the prior art "store and forward" procedures described in the '080 patent. A* 48.

4. The '954 Patent

i. "host"

Once again, Fore improperly seeks to limit a general claim term, arguing that a "host" is limited to "network end-user devices." F. Br. at 54. Fore is wrong. A "host" is simply a participant in a multicast. Claim 9 does not limit "hosts" to only network end-user devices, nor, for that matter, does the '954 patent specification. Nor is there any reason to exclude switches, bridges, routers, or gateways from the definition of host, as Fore proposes.

[18] Fore also incorrectly asserts that Claim 6 requires one source address list per spanning tree. (F. Br. at 44). This is another attempt by Fore to improperly limit the claim to the embodiment in the specification and to modify the claim terms. Claim 6 merely recites a correspondence between the source address lists and the number of trees supported by the gateway, but does not limit the correspondence, and certainly does not require a one-to-one mapping of source address lists and spanning trees. Moreover, contrary to Fore's assertion, claim 6 does not require a gateway to create more than one spanning tree. F. Br. at 42. Claim 6 simply requires multiple spanning trees for the network.

ii. "packet"

Here again, Fore attempts to read a narrowing limitation into the general term "packet," asserting that a "packet" is a data packet that is destined to a multicast address and that carries data for network end-users participating in the multicast. F. Br. at 55. The claim term "packet," however, is plainly not so limited. "Packet" includes all types of packets, including, but not limited to, data packets and control packets.

In attempting to support its argument, Fore also improperly relies on extrinsic evidence in the form of deposition testimony. Such testimony "may only be relied on if the patent documents, taken as a whole, are insufficient to enable the court to construe disputed claim terms. Such instances will rarely, if ever, occur." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1585 (Fed. Cir. 1996). This is not such an instance. The term "packet" is not ambiguous. The Court "must presume that the terms in the claim mean what they say, and, unless otherwise compelled, give full effect to the ordinary and accustomed meaning of claim terms." *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 989 (Fed. Cir. 1999). The ordinary and accustomed meaning of "packet" includes both data and control packets.

iii. "first host"

The "first host," is not limited, as Fore contends, to the "initial" host that sends a packet to the multicast address before any other host. "First," as used in the claim, does not mean first in time. Rather, use of the word "first" is a common claim drafting technique to distinguish between two similar items, such as between two groups of hosts, "first hosts" and "other hosts." *See, e.g.*, Farber, "Landis On Mechanics Of Patent Claim Drafting," p. III-15, Fourth Edition (December 1998) (Ex. Q, A*181). Fore deliberately distorts this common construction, again, to advance its noninfringement position.

Moreover, the method steps of claim 9 do not necessarily begin before any host has transmitted a packet to the multicast address. Rather, these steps can also be found in the middle of a multicast operation.[19]

It follows then that Fore's second assertion on this point, "that the initial data packet sent by the first host to the multicast address must reach all packet switches in the network and all hosts connected to those packet switches," (F. Br. at 58-61) is also incorrect. In the example introduced in footnote 19, where C is considered the "first host" in Figure 3, the multicast packet sent by C will not reach packet switch 3 or host B because there is no table entry in packet switch 2 for trunk 2. Therefore, Fore's strained assertion that a multicast packet sent by the "first host" must reach every packet switch and host for the claimed invention to be operable is wrong and contradicts the very teaching of the '954 patent.

Fore's argument of inoperability fails even under its own example, Diagram 9 of its brief. That example simply illustrates that the method of claim 9 causes the packet switches to broadcast multicast packets until the packet switches learn who the multicast participants are and what network resources are required to transmit multicast packets to the participants. Thus, this example shows that claim 9 is working properly.[20]

Moreover, Fore simply ignores the prosecution history of the '954 patent in advancing this argument. As originally drafted, this limitation read "transmitting a packet addressed to a multicast address from a first host to **all** packet switches in said network." During prosecution, the applicants amended claim 9 by deleting the term "all" and replacing it with "**a plurality of.**" Ex. O, A*155

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[19] For example, in the multicasting illustration of Figure 3 of the '954 patent, if at some time after host A transmits a packet to a multicast address, host C is considered the "first host" and hosts A, B, D, and E are considered "other hosts." Accordingly, in this instance the "first host" was not the first to send a multicast packet.

[20] Fore's operability argument also fails for the reasons discussed above in section II.B.4.

(emphasis added). Just as claims "may not be construed one way in order to obtain their allowance and in a different way against accused infringers, *Southwall Tech., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995), neither may Fore advance a claim construction erasing the amendment replacing "all" with "a plurality of." It has long been the rule that "[a]llowed claims may not be construed to have the same meaning which they would have had without amendment." *Straussler v. United States*, 290 F.2d 827, 831 (Ct. Cl. 1961).

iv. "transmitting further packets"

Fore asserts that the claim 9 step of "transmitting further packets" requires a table with a timer entry. Claim 9 says nothing of a timer entry in a table. Here again, Fore improperly tries to read additional, structured limitations into claim 9, attempting to limit its scope.

Fore's construction of claim 9 requires all packet switches in the network to maintain the table defined in claim 9. This construction is wrong for several reasons.[21] First, as previously explained, this interpretation contradicts the operation of the disclosed embodiments. This is illustrated in Figure 3 of the '954 patent, where neither packet switches 3 nor 7 have a table, but the method is implemented.[22] Second, packet switches that do not implement the method of claim 9 can still be operable when, for example, the packet switch broadcasts the received multicast packet, which as explained in the Background of the '954 patent, was a capability of packet switches in the prior art.

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[21] Fore attempts to read the term "all" once into claim 6 of the '080 patent, and twice into '954 patent claim 9. Fore's repeated attempts at the same argument reveal Fore's motives in trying to narrow claims to advance its noninfringement position.

[22] Co-inventor, Stuart Feldman's deposition testimony covering the operation of the preferred embodiment is irrelevant to this argument. Fore's quotation from the Sincoskie and Cotton article concerning passive listening is also irrelevant because claim 9 is not limited to listen-only-multicast.

III. CONCLUSION

For all of the foregoing reasons, Bellcore respectfully requests that the Court construe the claims in the manner set forth above and in Bellcore's opening brief. Bellcore's claim interpretations are summarized for the Court's convenience in claim chart form, attached as Ex. P, A*158-178.

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Date: September 9, 1999

EXHIBIT 40

IN THE UNITED STATES DISTRICT COURT

IN AND FOR THE DISTRICT OF DELAWARE

- - -

BELL COMMUNICATIONS RESEARCH, INC., now TELCORDIA TECHNOLOGIES, INC.,	:	CIVIL ACTION
Plaintiff	:	
v.	:	
FORE SYSTEMS, INC.,	:	
Defendant	:	NO. 98-586 (JJF)

- - -

Wilmington, Delaware
Thursday, March 23, 2000
1:04 o'clock, p.m.

- - -

BEFORE: HONORABLE JOSEPH J. FARNAN, JR., U.S.D.C.J.

- - -

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PROCEEDINGS

(Proceedings commenced at 1:04 p.m)

THE COURT: Good afternoon.

(Counsel respond "Good afternoon, your Honor.")

MR. HERRMANN: Good afternoon, your Honor.

THE COURT: Good afternoon.

MR. HERRMANN: Your Honor has met Vince Kovalick before in this case, but your Honor has not had the opportunity, and I'd like to introduce Richard Smith from the Finnegan Henderson firm as well.

THE COURT: Good afternoon.

MR. HERRMANN: As well as Frank DeCosta and Matthew DelGiorno.

THE COURT: Good afternoon.

MR. MARSDEN: William Marsden for Fore Systems, Inc.

With me from our San Diego office today are John Gartman and Chris Marchese. John and Chris will be doing the argument today on the claim construction issues.

Also here from our San Diego office are Todd Miller and Shekhar Vyas.

From the client, your Honor, John Dials.

And also seated in the front row, we have two experts who are available to answer questions if the Court may have them. Doctor Ian Leslie, who is Chairman of the Computer Science Department at the University of Cambridge in England, and Dr. Larry Wittie, who's Professor of Computer Science, State University of New York, at Stonebrook.

THE COURT: Good afternoon. Ready to begin?

MR. KOVALICK: Thank you, your Honor.

Your Honor, this is Mike Arrington from our firms. If it's okay, he's going to work with the boards?

THE COURT: Sure.

MR. KOVALICK: Just to complete some of the introductions, we have from Telcordia Bruce Sidman.

We also have our experts if you have any questions for experts.

We have Dr. Misha Schwartz on the left.

THE COURT: Good afternoon.

MR. KOVALICK: We're also going to split our presentation. We'll split it up two patents apiece. And, as you know, the four patents in this litigation relate to telecommunications. I know you're familiar with telecommunications having recently done the Lucent and Newbridge litigations, so some of the concepts will be familiar to you I'm sure.

We have, however, prepared a little bit of animation to kind of help out with some of this. Understand some of the concepts. If I can just give you a little bit of an introduction, this is telecommunications technology and it basically involves networking. So we've set up kind of a fictional network, but it's fairly realistic. It involves kind of a hospital campus where one might want to connect up multiple buildings in a hospital campus. You have surgery, classroom and an admin. The switches would be colored nodes or messaging devices for sending messages around.

On the left you'll see where we're going to multiplex signals from various input devices. We're going to bring them into the systems, get them out in the network and distributed in and throughout these buildings. This is kind of a partial look at a network. It could be larger than this. It could be buildings on the other side of the street. We'll concentrate on this. We're going to use this to kind of focus on where the inventions are, give you some help in seeing where they fit into networking technology today.

If I may just very quickly review the rules that we used in our claim interpretations, I think that they're pretty standard. The Court is obviously aware of them. The rules of claim construction, first of all, a

tells you that's elaborated in Figure 4 of the patent.

So here these three sources go into the DTDM assembler. The assembler is the train that generates the train of empty frames. These things basically get packetized and stuffed into that train of empty frames. As we saw in the last picture, the train of empty frames now becomes a train of frames, some of which are not empty. That's what you see coming out here (indicating).

The next item in the block is called a DTDM MOX and it's to be distinguished from a DTDM assembler. The DTDM MOX, as you now know, has as one input what I will call a sparsely-populated frame train. Sparsely populated means some of the payloads for some of the frames are filled with packets, but as we saw in the last figure, some are not.

And so this DTDM MOX has on its input lots of sparsely populated frame trains. And the DTDM MOX concentrates those sparsely-populated frame trains into another train of frames, which is now more densely populated.

So basically from left to right you see concentration.

This last thing is called a TDM assembler. The patent does not focus on this at all in terms of the claims. There are a lot of Bellcor patents that

derive from this application, but this TDM assembler essentially concentrates the data a little bit more than the DTDM MOX does.

Then it goes out onto the network out here and ultimately comes back. That's what this arrow is showing. And every block on the bottom more or less performs the inverse function of every one of these blocks on the top. So the first one here does the inverse of the one above it. The one here takes a very densely-poopulated frame train and makes it into sparsely-populated frame trains.

And then on the very bottom you'll see the DTDM disassembler, which takes that sparsely-populated frame train and separates it out into video and voice and data. And that's how you get the video packets that I was sending to you.

So that's the big picture, so to speak.

I will run through some of the little pictures, or the blowups of these items on the screen. I will tell you up front that the ones that are important in this case are the blow up here (indicating). This one is not, frankly, important (indicating). Maybe there will be a dispute over that, but I will tell you that's our view. This one is not very important. This one is not very important. This one is not (indicating). And

this one is not (indicating).

You can see there is Figure 12, which Mr. Smith spent a lot of time talking about. Figure 12 is imbedded in almost every one of these. There's a typographical error up here (indicating), on that one. Figure 6 does not have a Figure 12 and 7 and 8 as I recall it does. So just note that in your notes if you are taking any.

All right. So the focus of our presentation will be on Figure 4. So let me go to Figure 4 and talk about it. And let me go back quickly first.

Let's look for just one second again at what Figure 4 is doing for us. It is going to create a train of empty frames. It is going to then receive data from three sources, and it is going to put -- it's going to packetize that data and it's going to put it into the payload areas of those empty frames. So that's what this next figure should be showing you. And it does.

All right? So here's Figure 4. This box right here, this framer 52 (indicating), is what generates the train of empty frames. I will elaborate on that later and I will show you how it does it.

So framer 52 generates a train of empty frames. There is a serial data output of that framer. You can see it. It's labeled SDO. The train of empty

frames goes into a block here. This whole thing is like an interface. This one down below is an identical interface. This interface you can see has a data input. This, for instance, is your video conference equipment. Your video conference equipment might send its data here. It gets packetized here. It gets held up here, which is basically a memory. And then it goes into another framer.

Now, look. This framer is labeled 53. This one is labeled 52. There's a difference between these two. They're both shown in Figure 12. The text explains Figure 12, will tell you that that Figure 12 figure -- that Figure 12 can do multiple things. One is that it can generate a train of empty frames and that's what it's doing in figure -- in the figure here, where it's labeled 52. It can also do additional things. It can receive a train of empty frames from another framer. And it can insert packets, such as from here (indicating) into empty payloads.

It can also receive, as in this case down here on 53, a train of frames (indicating) from an upstream framer, some of which may be empty, and some of which may be filled. And so this framer 53 down here basically takes incoming frames. It looks into the overhead area of the frame.

- - -

MR. GARTMAN (Continuing): What it does is it asks the overhead, Are you empty or are you full?

And if the answer is, I'm full, then this framer just passes that thing on down the line, because it can't stick information in a full frame.

On the other hand, if when it checks the overhead --

- - -

MR. GARTMAN (Continuing): On the other hand, if, when it checks the overhead it's, I'm empty, framer 53 down here might actually put a packet in that empty payload area if it has a packet. It may not. There may be no data coming from over here. That's basically how Figure 4 works.

As I promised, I was going to show you framer 52 and framer 53. Actually, my slide show here, I'm going to blow through it. I was going to actually illuminate what these other figures are. I don't see that as being necessary any more, given the way the discussion has gone today, but I'm happy to answer questions about them if the Court would like to go back.

I want to go now to Figure 12. So before I do that, I want to put you back in the context of Figure 2, because I think that you can mentally correlate Figure 2 now to what you've seen in Figure 4. You can see the

empty frames here and you know how they're generated. You can see the three sources. You can see the packetizers. You can see the packets. And now you know actually how because you've seen interface on that last diagram. You can see how these packets actually get stuffed into empty payload areas if there are empty payload areas available.

So here's Figure 12. And I think we'll probably have a lot to say about Figure 12.

Here's how it works. It does two things or can do two things. In the -- one of the two things that it can do, as I said earlier, it can generate a train of empty frames. That is the box labeled 52 at the top, Figure 4. When it does that function, and if you look at the specification of the prosecution -- of the patent, it will show you two very discrete sections of text, what it says in the first one, when it's doing the empty frame generation and the other one, when it's doing something else, which I will get to.

But let me focus on the empty frame generation. When this thing is generating empty frames, parts of it are not used. The text of the patent says so.

Okay. Let's see. You need to read it out loud. Basically, what it says is, when this framer unit 200 -- you see the number 200 up there -- this is the

second part of the packet testify, where it's saying it may also be used to generate a train of empty frames. It describes how it does it. It says this frame bright ROM -- maybe I can find that. Frame byte ROM reads out the overhead portion of the frame. How does it do that? Reads it out.

I will agree with Mr. Smith, that it's an eight readout from this ROM. I don't think that's relevant, but I agree with that. It reads it out in eight bits. It goes through this Tri-State gate. Goes up this bus here. And then, what I think is important, is that overhead is converted from parallel to serial so that when this thing is operating as a generator of frames with empty payload yields, the text of the patent will say, there is no serial data on the input, there is nothing on this input. The only thing it does is read out the overhead in the form of a serial bit screen. That's important because that's language that's in the patent claim, and the patent claim talks about a serial bit screen.

So what you see, when this thing is generating empty frames, it generates a serial bit frame -- bit stream that has overhead every so often and then an empty payload field. And that's exactly what's shown in Figure 2 and that's exactly what's shown in Figure 4, which I

went through previously.

Now, if you remember Figure 4, there was an empty frame generator up at the very top. It had an SDO output. Remember that. That's the same as this serial data output (indicating). And so what you saw in Figure 4, the upper right-hand corner, was the block 52, which generates a train of empty frames. And this is exactly how it does it. There's no input to it. You can go back to Figure 4 and confirm that there's no input to it so there can't be any packets stuck in there because there's no input to it when it acts as an empty frame generator, and the text of the patent says that.

So it serves another function as well. I'm getting to that one now. And that is as you saw in Figure 4, immediately under the block labeled 52, there was another framer labeled 53. That framer 53 does have an input, because it comes from the empty frame generator. And so the empty frames, which framer 52 generate, become the serial data input to the downstream framer.

The downstream framer, of course, has two inputs. It receives the serial train of empty frames from framer 52 and it also receives packets, such as, for example, from your video equipment.

So the train of empty frames can come in on the serial data input up here, and your video equipment

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is, there's a serial stream that comes out here. It's a serial bit stream. It's SDO. That means serial. That is a train of empty frames when it comes out of framer 52 (indicating). And it goes into 53 and, yes, at some point in 53 there are some things converted from serial to parallel and vice-versa, all of which in our opinion is irrelevant. It comes out and the claim, the only time we're debating the significance of the claim is when it says there's a serial bit frame, and I'm paraphrasing here, that is a train of frames with empty payloads. And there's no question that that exists in this patent. It's right there (indicating). Comes out right there.

I will now go to the next point. I hope I'm not repeating myself. But this is the limitation where we believe the claim does, in fact, require multiple frames to exist with empty payload fields. It says a sequence of frames, each of them having a transmission overhead field, which I'm not talking about at the moment, and an empty payload field, a sequence. Each of them has an empty payload field.

Here's our proposed construction for that. You can see the difference. And although I can't ask the Court to do anything really, I would appreciate it perhaps if we can focus on what Bellcor has said in their brief. A complete, empty frame never exists before a packet has

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an opportunity to be inserted. The disclosed circuit in no way generates complete, empty frames.

Well, they're here in Figure 2. Of course, that's now turned into a -- I forget the terminology. Conceptual diagram, or something like that.

The patent specification does not say that. The patent specification treats Figure 2 with as much respect as any other figure in the patent. There's nothing about this being some hypothetical diagram or some conceptual diagram that's not to be implemented.

Furthermore, here is the text again, which conclusively shows from the spec that this framer here generates a train of empty frames. I don't think it could be any more clear. And I've already shown in Figure 12, in fact, how that framer circuit generates that train of empty frames, and there has been some dispute as to whether it's parallel or serial. And when certain pieces of it come out of this ROM, indeed, this is -- the output of this, when that circuit is used as an empty frame generator, is a serial bit stream.

Furthermore, the prosecution history requires our result. Here's an excerpt from it. This was Bellcor's comments when they were distinguishing one of the references that was cited against the pending claims. Note the terminology here first. It's hard to see. I

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apologize for that. We probably would have chosen a different color. It says first generating a bit stream comprised of frames with empty payload fields. Then inserting into the empty payload fields.

In fact, I think if you look at the history of the briefing in this case, even Bellcor used to agree with us that empty frames were generated, because this is a quote from their opening Markman brief: Every frame entering the first interface 50 is empty. And if you can't have empty frames, this language does not make a lot of sense.

So that's our proposed instruction, your Honor, for the previously highlighted element.

Let me go to the next one. Partially overlapping. Here I'm focusing on empty payload field, and I think if the Court carefully looks at the briefing, you'll see that there's not only a dispute as to whether or not there are empty frames that are generated and a dispute as to whether or not there are multiple empty frames generated -- and by empty frames, sometimes the patent actually uses that phraseology. What's truly meant is a frame with an empty payload field, but that's sort of a shorthand, I think, that's used interchangeably in the patent.

But there's also a dispute as to what it

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means to be empty in the sense of the payload field. Is there -- and I think -- I think this is the dispute. We believe empty means zero data. And I -- if I try to paraphrase what Bellcor is saying here, the dispute seems to be they believe the frame is empty if it has no source data in it, but that leaves open the option that there could be some other kind of data in it, and it would still be empty, which we disagree with.

Now, we don't know what source data means in this context, but our position is simply that if it has data in it, source data, whatever, it's not empty. If it has no data in it, it is.

There's a history behind this phrase. It's important. It's not trivial. It was added to avoid prior art there, the three -- there are three claims that were amended there. The three claims that are in dispute. You can see in this amendment, which was a first amendment made in the prosecution history, the word empty was added to each one of them.

And just for the sake of clarity here, since some of my team pointed out it wasn't altogether clear, when I say emphasis on the original, in the Patent Office, when language is added to a claim, the rules, the Patent Office rules basically say you underline the newly-inserted language. So this is in the original,

EXHIBIT 41

REDACTED

EXHIBIT 42

REDACTED

EXHIBIT 43

REDACTED

EXHIBIT 44

REDACTED

EXHIBIT 45

REDACTED

EXHIBIT 46

REDACTED

CERTIFICATE OF SERVICE

I hereby certify that on the 25th day of October, 2006, the attached **REDACTED PUBLIC VERSION OF APPENDIX C IN SUPPORT OF TELCORDIA'S ANSWERING BRIEF IN PARTIAL OPPOSITION TO DEFENDANTS' MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,893,306** was served upon the below-named counsel of record at the address and in the manner indicated:

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